TSW14J57revE Firmware Design Document

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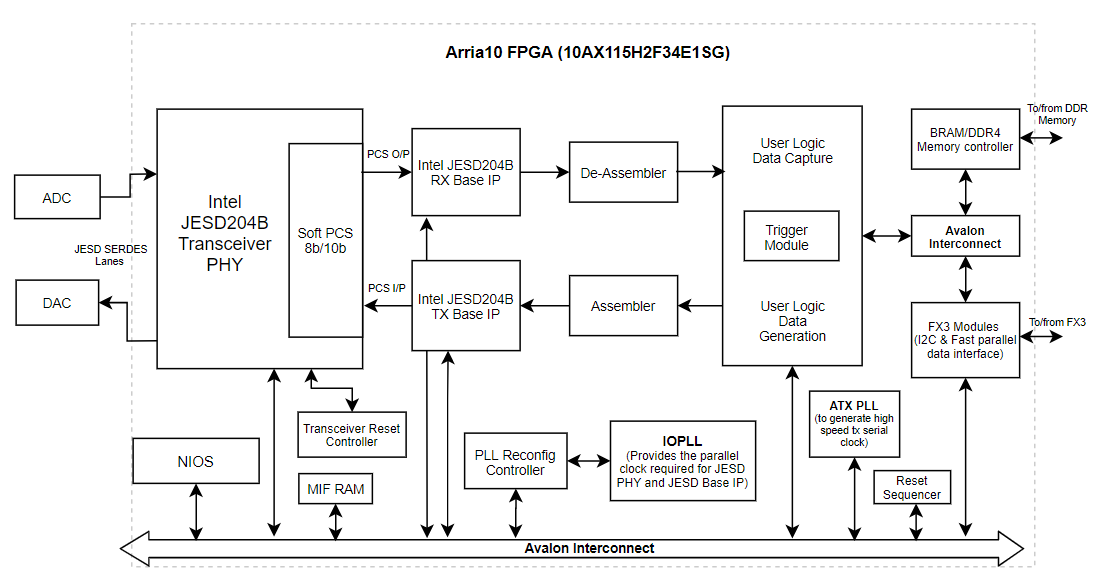
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# Overview:

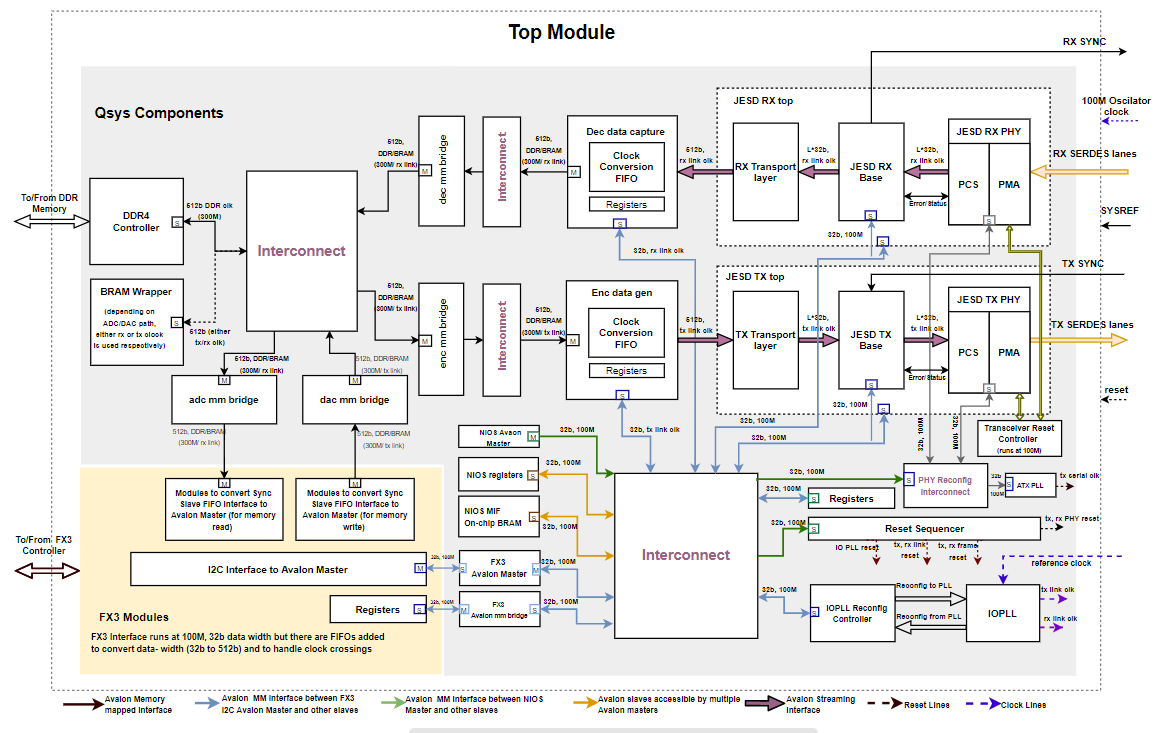
TSW14J57 is a hardware platform used to evaluate the performance of TI’s JESD204B devices. Examples of devices than can be used with TSW14J57 are ADC12DJxx00 family, ADC12J4000 and DAC3xJ8x family. The devices are evaluated by connecting their EVMs as daughter cards to the FMC port on TSW14J57 and using the HSDCPRO software to capture or send data. To enable TSW14J57 to work, the board includes a FX3 USB 3.0 controller, 16-Gb DDR4 SDRAM memory and an Arria10 GX 115 FPGA. FW builds are compiled with speed grade2 settings (yet to be modified) but the EVM has FPGA part of speed grade1. Inside the FPGA, there are interface controllers for connecting FPGA to DDR4 memory and other external peripherals. Also present are 24 high-speed SERDES transceivers of which 16 are used for interfacing to the data converter under evaluation, JESD204B IP, Reconfiguration controllers to dynamically switch between supported modes and PLLs for internal clock management. The firmware is compiled with Quartus Prime 16.1 Standard version software and needs Intel JESD204B license.

This document gives a detailed description of the FW modules and also lists the FW builds maintained with HSDC Pro

Major FW Blocks



Functional Block Diagram



# Quartus Tool Version:

FW source developed in Quartus Prime 16.1 Standard Version and requires Intel JESD204B version to recompile the design

# FW Architecture:

## JESD204B Interface:

Major modules involved in the JESD interface are the following, kindly refer the functional block diagram shown above to get a picture of the data flow between these modules

1. dec\_data\_capture\_gz - Data Capture Module

* Module has Status and control registers which HSDC SW uses through FX3 USB3.0->I2C->Avalon Memory Mapped interface. There is an FSM to execute the ADC capture process based on the register values set by HSDC SW.
* During capture, it receives 512bit valid JESD data from RX transport layer (altera\_jesd204\_deassembler) through Avalon Streaming interface and writes the same to DDR4 external memory or to BRAM through Avalon Memory Mapped Interface.

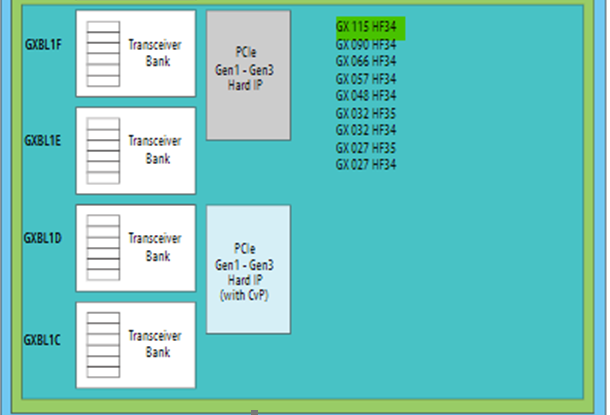
1. enc\_data\_gen\_gz- Data Generation Module

* Module has Status and control registers which HSDC SW uses through FX3 USB3.0->I2C->Avalon Memory Mapped interface. There is an FSM to execute the DAC Send process based on the register values set by HSDC SW.
* During Send, it reads 512b valid data from either DDR4 external memory or BRAM through Avalon Memory mapped interface and transfers the same to TX transport layer (altera\_jesd204\_assembler) through Avalon Streaming interface.

1. jesd\_top\_con- Wrapper for jesd\_rx\_top, jesd\_tx\_top and jesd\_clk\_rst\_gen modules
2. jesd\_rx\_top- holds the RX JESD204B Base and PHY IP instances and RX transport layer to buffer JESD data, forms 512bit words before passing to data capture module
3. jesd\_tx\_top- holds the TX JESD204B Base and PHY IP instances and TX transport layer to buffer the 512bit words received from data generation module and sends only the data required for active SERDES lanes
4. jesd\_clk\_rst\_gen- Has the IOPLL instance (jesd\_io\_pll), generates TX and RX frame clocks and its associated resets

### JESD204B TX/RX PHY IP:

JESD204B PHY IP uses Arria10 transceivers for the high speed communication with ADC or DAC devices. There are 24 transceiver channels in the Arria10 FPGA part available in TSW14J57revE EVM and the layout of the same part GX115 HF34 is highlighted as below. The channels are placed in 4 banks of 6 each. The reference clock from bank 1C (FMC pins D4/D5) is used to source itself and upper 2 banks covering 18 transceiver channels in firmware. Note that we are using only 16 of them in design (only 16 routed from FMC as well)



JESD PHY IP has two major blocks Physical coding sublayer (PCS) and Physical Media Attachment (PMA). PCS layer can be either hard logic or soft logic, soft PCS option is used in the design to support higher data rates. Intel Transceiver reset controller IP is used to handle the analog and digital resets of PHY IP.

PHY layer operates with two clock domains, high speed serial clock and parallel link clock. In case of RX, serial clock is recovered by the clock data recovery block (CDR) of transceivers. In case of TX it is sourced by the ATX PLL which can be reconfigured dynamically from HSDC software for different data rates. The link clock (both tx/rx link clock) comes from an IOPLL which is reconfigured run-time to get data rate/40 clock always. By default, JESD PHY IP is compiled with following settings, but it can be configured dynamically from HSDC software for different data rates through NIOS II on-chip soft processor. NIOS is coded to receive commands from software and carry on the reconfig process.

Default RX PHY IP Settings: data rate- 15000Mbps, CDR Reference clock- 375M

Default TX PHY IP Settings: data rate- 15000Mbps

We have four instances of JESD PHY IP in the design each handling 4 lanes. It is possible to use 2 PHY IP instances each handling 8 lanes, there is no specific reason not to use this way. Since most of the modules were ported from J56, it was not modified.

The default PMA settings of PHY can be changed by streaming MIF files. These files are generated for different lane rates and available in HSDC software in below folder for dynamic reconfiguration purpose. To start reconfiguration, software first writes the contents of MIF file to on-chip RAM and then triggers NIOS with reconfig commands

\\*HSDC Pro Installed directory \High Speed Data Converter Pro\14J57revE Details\MIF Files

Default Directory: C:\Program Files (x86)\ Texas Instruments

### JESD204B TX/RX Base IP:

JESD IP can be used in duplex mode (Base & PHY together) but we have used Base and PHY separately in Simplex mode in the design. This was done because in duplex mode, parameters like csr\_lane\_polarity (to perform SERDES P/N Swapping) were not exposed in duplex mode.

JESD Base IP takes care of CGS and ILAS phase of the de-serialized data either received from or sent to JESD PHY IP. The IP core has a number of internal registers that needs to be configured to enable it to work with J57 platform. These registers are accessible through Avalon Memory Mapped (MM) interface. In TSW14J57, the registers are programmed through the FX3 I2C -> Avalon MM interface from HSDCPRO software. It also reconfigures JESD configuration values (LMFSK) run-time to support different JMODEs. HSDC software reads the required config values from device initialization (Ini) file and writes them to the registers. INI files are available in below path

\\*HSDC Pro Installed directory \High Speed Data Converter Pro\14J57revE Details\ADC files

\\*HSDC Pro Installed directory \High Speed Data Converter Pro\14J57revE Details\DAC files

Input/output of the JESD Base IP is of 32bit data width per lane and operates at data rate/40 clock (known as link clock) and uses Avalon Streaming Interface. The link clock is sourced by an IOPLL in design which is reconfigured run-time such that it is always data rate/40 irrespective of the reference clock input. The data coming out of the RX JESD IP is formatted in Transport layer and is then stored in either DDR4 or BRAM memory. Similarly data read from either DDR4 or BRAM memory is formatted in Transport layer before sent to TX JESD IP. By default, single IP instance supports maximum of 8 lanes and to support 16 lanes two IP instances are used in the design. The firmware is compiled with below LMFSK and reference clock settings which can be changed dynamically through the Avalon MM interface and by configuring IOPLL link clock output respectively

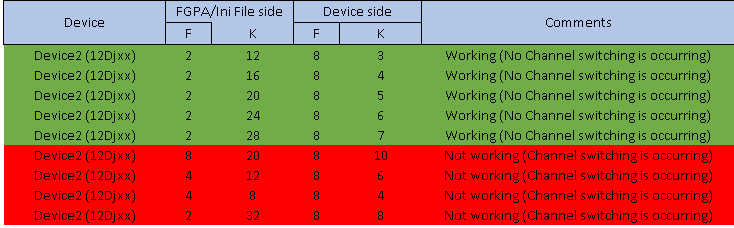
Default RX BaseIP Settings: LMFSK- 841120, Scrambling- 0, Link clock- 375M, Data rate- 15000Mbps

Default TX PHY IP Settings: LMFSK- 841120, Scrambling- 0, Link clock- 375M, Data rate- 15000Mbps -

|  |  |  |
| --- | --- | --- |
| **Signals** | **FMC Pins** | **FPGA Pins** |
| Reference clock | D4/D5 | AD28/AD27 |
| TX SYNC | F10/F11 | C27/B27 |
| RX SYNC | G12/G13 | B23/C23 |
| TX ALT SYNC | F19/F20 | C24/D243 |
| RX ALT SYNC | H31/H32 | B26 (LVCMOS-1.8V)3 |

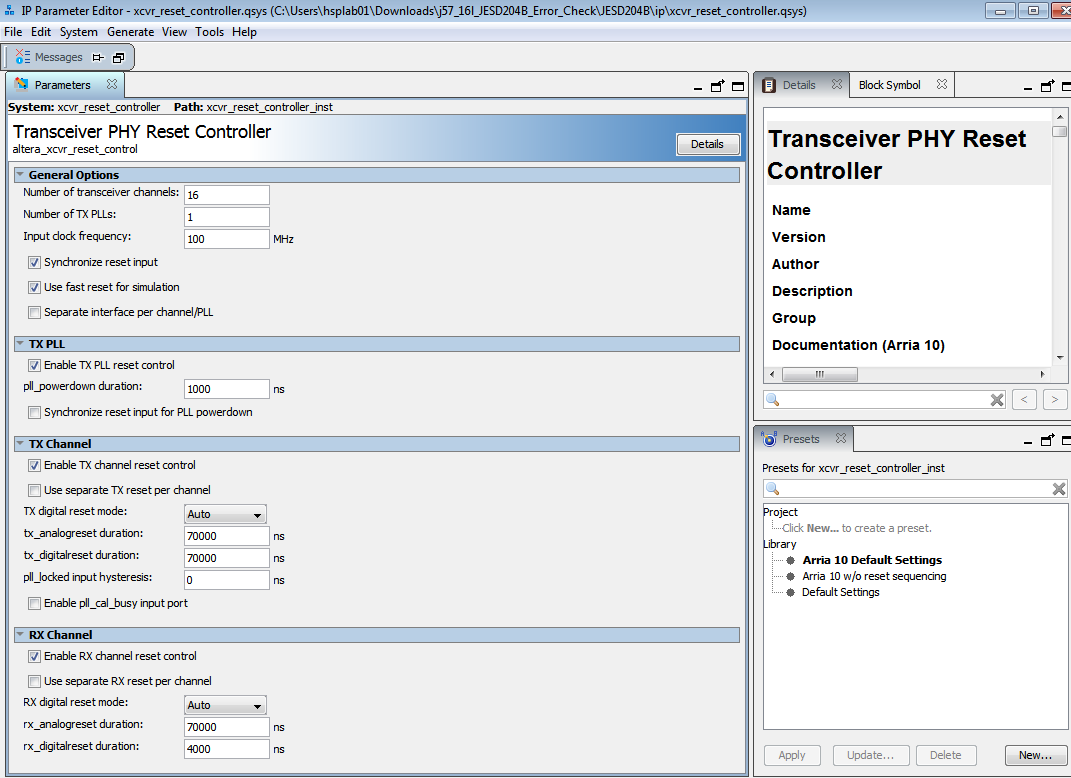
**Limitations:**

1. Intel JESD204B Base IP version available with Quartus 16.1 software doesn’t support F=3 mode. Also we observed SOMF (start of multi-frame signal from the JESD Base IP) mis-alignment issues with F=8 or when number of lanes=1. We haven't tested with the latest Quartus versions that Intel released
2. To fix these special cases, work-around was to set F & K differently in FPGA IP than what is set in device and only the product (FxK) value multi-frame alignment is ensured to match between device and Firmware. Some combinations of F&K caused SOMF signal mis-aligned which in turn caused channel swapping in the device side, please refer below for the values which worked, this was tested with ADC12DJ3200 F=8 modes
3. With the work-around, we can get good ADC captures and DAC generation. Note we have to disable the frame alignment alarms set in DAC GUI as the frame boundaries will not match as F values are mismatched between device and FPGA. In some cases, we had need to disable the lane/frame alignment character generation in the JESD IPs in firmware. Disable feature works only in the TX JESD Base IP and we couldn’t disable alignment character checking in the RX JESD IP



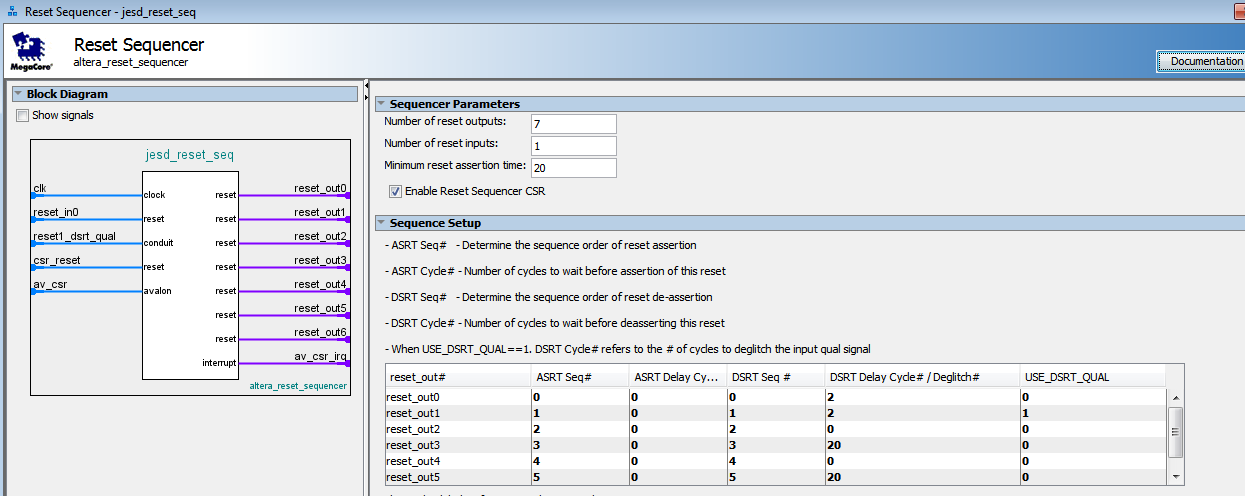
### Transceiver Reset Controller:

The design uses Intel’s Transceiver Reset Controller IP to reset the transceiver channels of JESD PHY IP both TX and RX. It controls both analog and digital resets and resets all 16 transceiver channels together not individually. Below is the IP settings



### Reset Sequencer

The design uses Intel’s Reset Sequencer IP to sequence assertion and de-assertion of IOPLL, transceiver, link and frame resets used in firmware. This IP is controlled by NIOS through Avalon MM interface. There are 7 reset signals out of this IP and it uses one reset de-assert qualifier. The qualifier is ‘IOPLL locked’ status and is used to de-assert tx PHY resets. The seven reset outputs are IOPLL reset, tx PHY reset, rx PHY reset, tx link reset, tx frame reset, rx link reset and rx frame reset and they are de-asserted in the same order with certain delay. Also it can be controlled individually by NIOS. The settings of reset sequencer is as given below



### Transport Layer

Rx transport layer (altera\_jesd204\_deassembler) receives 32bit data per lane from the JESD Base IP for every link clock, buffers the same to form 512bit data aligned with Start of multi-frame (SOMF) and sends the same to capture module ‘dec\_data\_capture\_gz’ through Avalon Streaming Interface. JESD IP can operate with any number of active lanes (from 1-16) depending on the JMODE, but the transport layer always sends 512 bit data out of it. This is implemented using shift registers and counters the threshold of which is based on ‘L’.

For example if the active lanes L=4, for every link clock (lane rate/40 clock), transport layer receives 32bits per lane, so 128bit every clock. This gets buffered and in 4 clocks, we have 512bit data which can be shared to data capture module. The Valid signal of Avalon Streaming interface is asserted once in every 4 clocks so the capture module receives valid 512bits and operates with it. Data format of JESD Base and the packing done in RX transport layer for L=4 case is shown below and the same is buffered for 4 consecutive clocks to form 512bits

TX transport layer (altera\_jesd204\_assembler) receives 512b data from data generation module ‘enc\_data\_gen’ through Avalon Streaming Interface, sends out 32bit data per lane aligned with SOMF to the JESD Base IP on all active lanes. This is implemented using shift registers and counters the threshold of which is based on ‘L’.

Considering L=4 case, out of the 512bits received from data generation module, 128bits are sent to JESD base per clock and transport layer asserts ready signal in Streaming interface only once for every 4 link clocks. Data format between the JESD Base and the packing in transport layer for L=4 case is shown below

Data Packing- Consider JESD RX Base to Transport layer

Data Packing- Consider TX transport layer to JESD TX Base

Tx\_sample\_data [0..127]

rx\_sample\_data [0..127]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **MSB** |  |  |  |  |  |  |  |  |  | **MSB** |  |  |  |
|  | M3S0  15..8 | M3S0  7..0 |  |  | JESD Base IP Data Format |  |  |  |  |  | M3S1  15..8 | M3S1  7..0 |  |  |
|  | M3S1  15..8 | M3S1  7..0 |  |  | **LMF- 442** | | | |  |  | M3S0  15..8 | M3S0  7..0 |  |  |
|  | M2S0  15..8 | M2S0  7..0 |  | **L3** | M3S0  15..8 | M3S0  7..0 | M3S1  15..8 | M3S1  7..0 |  |  | M2S1  15..8 | M2S1  7..0 |  |  |
|  | M2S1  15..8 | M2S1  7..0 |  | **L2** | M2S0  15..8 | M2S0  7..0 | M2S1  15..8 | M2S1  7..0 |  |  | M2S0  15..8 | M2S0  7..0 |  |  |
|  | M1S0  15..8 | M1S0  7..0 |  | **L1** | M1S0  15..8 | M1S0  7..0 | M1S1  15..8 | M1S1  7..0 |  |  | M1S1  15..8 | M1S1  7..0 |  |  |
|  | M1S1  15..8 | M1S1  7..0 |  | **L0** | M0S0  15..8 | M0S0  7..0 | M0S1  15..8 | M0S1  7..0 |  |  | M1S0  15..8 | M1S0  7..0 |  |  |
|  | M0S0  15..8 | M0S0  7..0 |  |  | [31,30,29,28………………3,2,1,0] |  |  |  |  |  | M0S1  15..8 | M0S1  7..0 |  |  |
|  | M0S1  15..8 | M0S1  7..0 |  |  |  |  |  |  |  |  | M0S0  15..8 | M0S0  7..0 |  |  |
|  |  | **LSB** |  |  |  |  |  |  |  |  |  | **LSB** |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

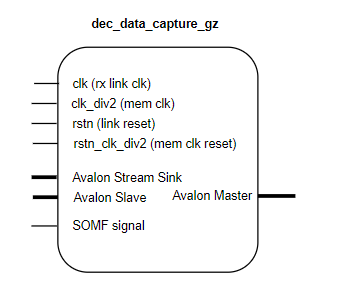
Please note that the first octet sent/received in JESD Base IP is MSB bits [31:24] and first bit sent/received in the IP is MSB bit [31]

**Limitations on L Value:**

There are only five counters to handle L= 1,2,4,8 & 16 whereas other L values are coerced into one of the counters. L=3 is coerced to 4 and L= 5, 6 and 7 coerced to 8 and 8<L<16 are coerced to 16

### Data Capture Module

This module ‘dec\_data\_capture\_gz’ receives 512b data from the RX transport layer at RX link clock and writes the same to DDR4 memory at DDR clock (300M) or link clock if BRAM is used. The module has a state machine to sequence capture operation and registers controlled by HSDC software. Data write happens only when ‘capture’ bit is set by the HSDC software for the user specified samples and once the ‘done’ bit is set in firmware, data write stops and the software starts to read captured samples. There is a FIFO to handle clock crossing between link clock and DDR clock. The interface is as shown below and the important signals are given in below table



|  |  |  |
| --- | --- | --- |
| **\*Offset Address** | **Size** | **Description** |
| **0x20000** | 32 | [0]- capture start  [1]- capture done  [3]- xcvr mode  [31:5] data length |

\*register address = offset address + base address, base address= 0x400000

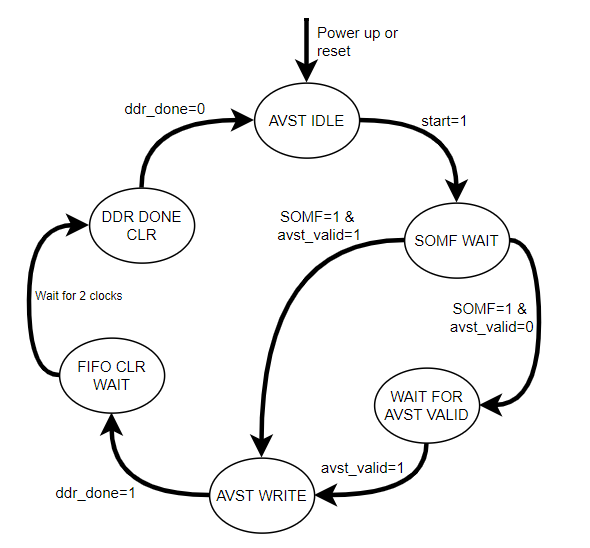
*Capture start*: when set high indicates start of data capture from JESD204B Base IP into the memory.

*Capture done*: This bit is set high when the length of data written to memory equals the user specified samples (value in the data length register). It indicates the end of data capture.

*Xcvr mode*: This bit puts the module in transceiver mode when set high. This is applicable only for DDR memory in which case memory usage is split between data capture and generation modules. Only half the memory is used for data capture and remaining half is used for data generation, so base address for data capture starts at 0 and base address for data generation starts at 0x1000000 (1GB)

*Data length*: sets the length of data to capture from the JESD204B IP and store in memory. The value of the data length register is given in terms of 512b words.

Following is the capture state machine implemented in dec data capture module.



As shown in above figure, at power up or reset, the State machine (SM) enters IDLE state. State machine moves to next state only when the conditions are met else stays in the same state

IDLE:

* Write enable signal to the FIFO and write enable to memory is held LOW
* Memory address counter is forced to zero

When the capture start bit is set to high, the state will transition from IDLE to SOMF WAIT.

SOMF WAIT:

* State machine waits for the SOMF pulse from JESD204B RX Base IP. It is used to align the start of data capture to the local multi frame counter that runs inside Base IP(LMFC)
* With SOMF being HIGH, if valid from the transport layer goes HIGH, FIFO write enable goes HIGH & data gets written. State moves to AVST WRITE
* If valid is LOW, state moves to AVST VALID and all the signals retain values from the IDLE state

AVST VALID:

* If valid from the transport layer goes HIGH, FIFO write enable goes HIGH & data gets written. State moves to AVST WRITE else stays in the same state

AVST WRITE:

* As long as valid from transport layer is HIGH, this state keeps writing data to FIFO.
* Once FIFO receives 256 words each of 512b, memory write request is issued and the memory address counter starts incrementing.
* Memory address counter is incremented in steps of the write burst size 8
* When the address counter reaches the value set in data length register, the capture done bit is set high to indicate the end of data capture and the state transitions to FIFO CLR WAIT

FIFO CLR WAIT:

* Reset to the intermediate FIFO is asserted and held HIGH for 2 clocks to clear its contents

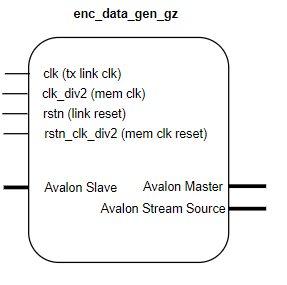
DDR\_DONE\_CLR:

* The state is added to clear the internally generated DDR done signal and de-assert the FIFO reset. State machine moves to IDLE from this state

### Data Generation Module

This module ‘enc\_data\_gen\_gz’ reads 512b data from the DDR4 memory at DDR clock (300M) or from BRAM at TX link clock, sends the same to TX transport layer at link clock. There is FIFO to handle clock crossing between DDR clock and link clock. It has a state machine to sequence Send process and registers controlled by HSDC software. Data gets played continuously on the TX SERDES lanes when ‘Send’ & ‘Loop’ bits are set HIGH by the HSDC software and it can be stopped with ‘Stop’ bit. The ‘Loop’ bit is set by default so data gets played continuously, to have a single shot (play only once) this bit can be set LOW, but currently single shot feature is not available

The interface is as shown below and the important signals are given in below table



|  |  |  |
| --- | --- | --- |
| **\*Offset Address** | **Size** | **Description** |
| **0x20000** | 32 | [0]- read start  [1]- read loop  [2]- read stop  [3]- xcvr mode  [31:4] data length |

\*register address = offset address + base address, base address= 0x0

*read start*: This bit is set high to trigger reading data from memory

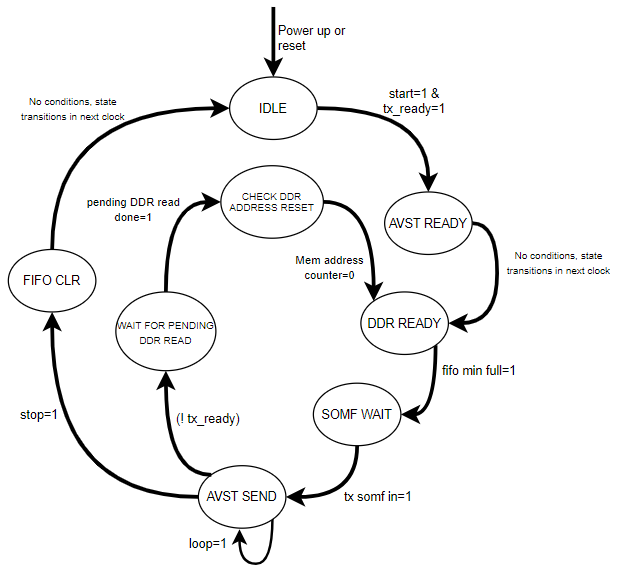
*read loop*: When set high forces the memory address counter to wrap around to zero. This puts the memory read operation in an infinite loop

*read stop*: when set forces the *enc\_data\_gen* module into idle state. In idle state, the address counter is reset to zero, read enable signals are de-activated and the data interface to the JESD204B IP holds the last data read from the memory.

*xcvr mode*: This bit puts the module in transceiver mode when set high. This is applicable only for DDR memory in which case memory usage is split between data capture and generation modules. Only half the memory is used for data capture and remaining half is used for data generation, so the base address for data capture starts at 0 and base address for data generation starts at 0x1000000 (1GB)

*data length*: sets the length of data to be read from memory that needs to be sent to JESD Base IP. The value of the data length register is given in terms of 512b words.

Following is the Send state machine (SM) implemented in enc data gen module. State machine moves to next state only when the conditions are met else stays in the same state



IDLE:

* FIFO is held in reset and Avalon data and valid of the Base IP streaming interface are held LOW
* Memory address counter is forced to reset
* When the ready signal from Base IP goes HIGH and read start bit is set by software, state moves to AVST\_READY and FIFO is out of reset.

AVST\_READY:

* In this state, read request to the memory is issued and FIFO starts getting filled. Memory address counter starts incrementing. It is incremented in steps of the read burst size 8
* State moves to DDR ready in the next clock.

DDR\_READY:

* Once the FIFO is filled with 64 words each of 512b, state moves to SOMF\_WAIT and AVST\_SEND\_DATA, else stays in DDR\_READY.
* Memory read requests are issued in parallel and the FIFO gets filled and the memory address counter keeps incrementing. Once the address counter reaches value set in data length register, it wraps to 0. As the loop bit is set, memory read requests will still be issued and data is read from base address again

SOMF\_WAIT:

* State machine waits for TX SOMF signal to move to AVST\_SEND state, else stays here

AVST\_SEND\_DATA:

* If the link ready signal from the Base IP is HIGH, read request is issued to FIFO and a counter keeps track of the read requests (FIFO reads counter). FIFO read back data and valid signal are assigned to the Avalon streaming interface of Base IP.
* Once the FIFO reads counter reaches value set in data length register, it is forced to 0 and the data gets played from the start again
* If the stop bit is set by software, FIFO reads counter is forced to 0, valid to Base IP is held LOW and state moves to FIFO CLR and the control register ‘0x20000’ is cleared
* Or if the link ready status is lost, state moves to WAIT\_FOR\_PENDING\_DDR\_READ

FIFO\_CLR:

* FIFO is held in reset and state moves to IDLE.
* Valid and data of the streaming interface retains the same value

WAIT\_FOR\_PENDING\_DDR\_READ:

* State machine moves into this state whenever the TX link is lost. In this state, memory address counter holds its previous value and a pending read requests counter updates as and when data is received from memory and no new requests are made.
* Until the pending requests are addressed, FIFO read requests are issued
* Once the pending counter turns zero, state moves to CHECK\_DDR\_ADDRESS\_RESET

CHECK\_DDR\_ADDRESS\_RESET:

* In this state, memory address counter is forced to 0 and state moves to DDR\_READY

### Trigger Module

Some of the J57revE FW builds support trigger feature- Hardware and Software based trigger modes for ADC capture is supported but SYSREF based trigger mode is not implemented yet. And none of the trigger modes are available for DAC generation. Trigger logic implemented in J57 is same as in J56 FW, please refer the ‘TSW14J56 RevD Trigger Modes.docx’, location linked in the references section. The document was made for J56 platform but the same FW modules are used in J57 FW

## NIOS II Soft Processor (Dynamic Reconfiguration)

NIOS II in FPGA takes care of the ATX PLL and JESD PHY IP dynamic Lane Rate Reconfiguration. NIOS is programmed to do specific tasks and has commands to execute each of them. Following are the list of NIOS commands that it uses to execute reconfiguration

To execute a specific command, HSDC Pro DLL writes to NIOS command registers through USB FX3-> I2C interface. In Firmware, I2C to Avalon master writes the values to on-chip RAM ‘Nios2\_reg\_ctrl\_bram’ (QSYS component). NIOS is programmed to read from ‘Nios2\_reg\_ctrl\_bram’ and decodes the command and proceeds as required

|  |  |  |
| --- | --- | --- |
| **S.No** | **Command Name** | **Description** |
| 1 | LANERATE\_RECONFIGURATION | Performs the steps required for the lane rate reconfiguration of ATX and transceiver (xcvr) channels using the loaded MIF files |
| 2 | USER\_CALIBRATION | Performs user calibration of ATX PLL and all transceiver channels |
| 3 | FORCE\_XCVR\_LINK\_FRAME\_RESETS | Asserts the xcvr, link and frame resets for all the links |
| 4 | RELEASE\_XCVR\_LINK\_FRAME\_RESETS | De-asserts the xcvr, link and frame resets for all the links |
| 3 | CHECK\_COMMAND\_INTERFACE | For Debug - To verify the command interface. The command data1 and command data2 will be displayed through JTAG-UART |
| 4 | CHECK\_XCVR\_READ\_INTERFACE | For Debug - Read data from Tx channel |
| 5 | CHECK\_XCVR\_WRITE\_INTERFACE | For Debug - Verify RMW for Tx channel |
| 6 | CHECK\_ATX\_PLL\_READ\_INTERFACE | For Debug - Read data from ATX |
| 7 | CHECK\_ATX\_PLL\_WRITE\_INTERFACE | For Debug - Verify RMW for ATX |
| 8 | CHECK\_FORCE\_RESET | For Debug |
| 9 | CHECK\_RELEASE\_RESET | For Debug - Release xcvr, link and frame resets depending on tx and rx phy |
| 10 | CHECK\_ARBITRATION | For Debug |

Each command has 5 registers- Command ID, Command Data1, Command Data2, Command Trigger and Status. Refer the Excel Sheet ‘NIOS2 Command Structure’ for more details, linked in the references section

### Reconfiguration Steps

To dynamically reconfigure ATX PLL and JESD204B PHY IP for different lane rates,

1. MIF files are generated for each of the targeted lane rates by changing the ATX PLL and PHY IP settings. These files are available in HSDC Pro Software in the following path of J57revE Details Folder

‘HSDC Installation Directory’\High Speed Data Converter Pro\14J57revE Details\MIF Files

Reference clock from the device is expected to be either lanerate/40 (x40) or lanerate/20 (x20) or x10 or x5 for different lane rates. The MIF files are generated and placed for all four clock ratios x40, x20, x10 and x5 and for different lane rates.

* MIF file for the JESD PHY IP (both TX and RX) get created automatically in below paths when the IP is generated with specific data rate settings-

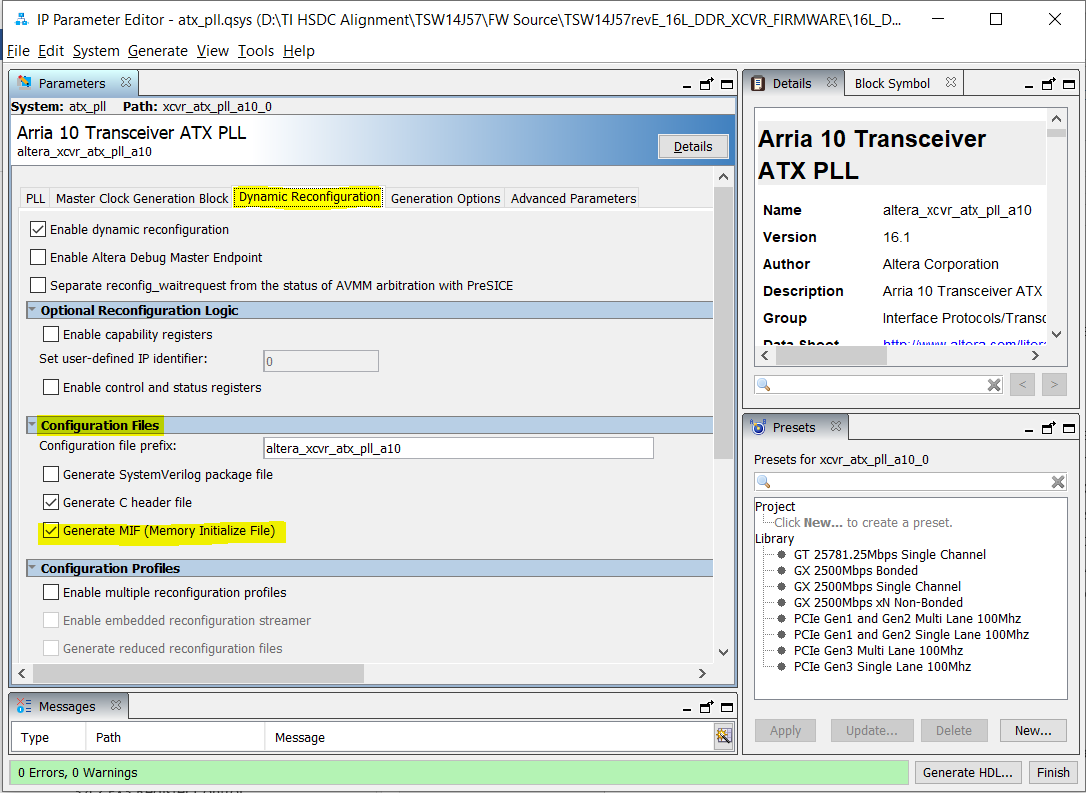
File Name: altera\_xcvr\_native\_a10\_reconfig\_parameters

\\*project directory\*\ip\xcvr\_jesd\_tx\altera\_xcvr\_native\_a10\_161\synth\reconfig

* MIF file for the ATX PLL gets created only when ‘Generate MIF’ option under the ‘Configuration Files’ section in ‘Dynamic Reconfiguration’ tab

MIF File Name: altera\_xcvr\_atx\_pll\_a10\_reconfig\_parameters

\\*project directory\*\ip\atx\_pll\altera\_xcvr\_atx\_pll\_a10\_161\synth\reconfig



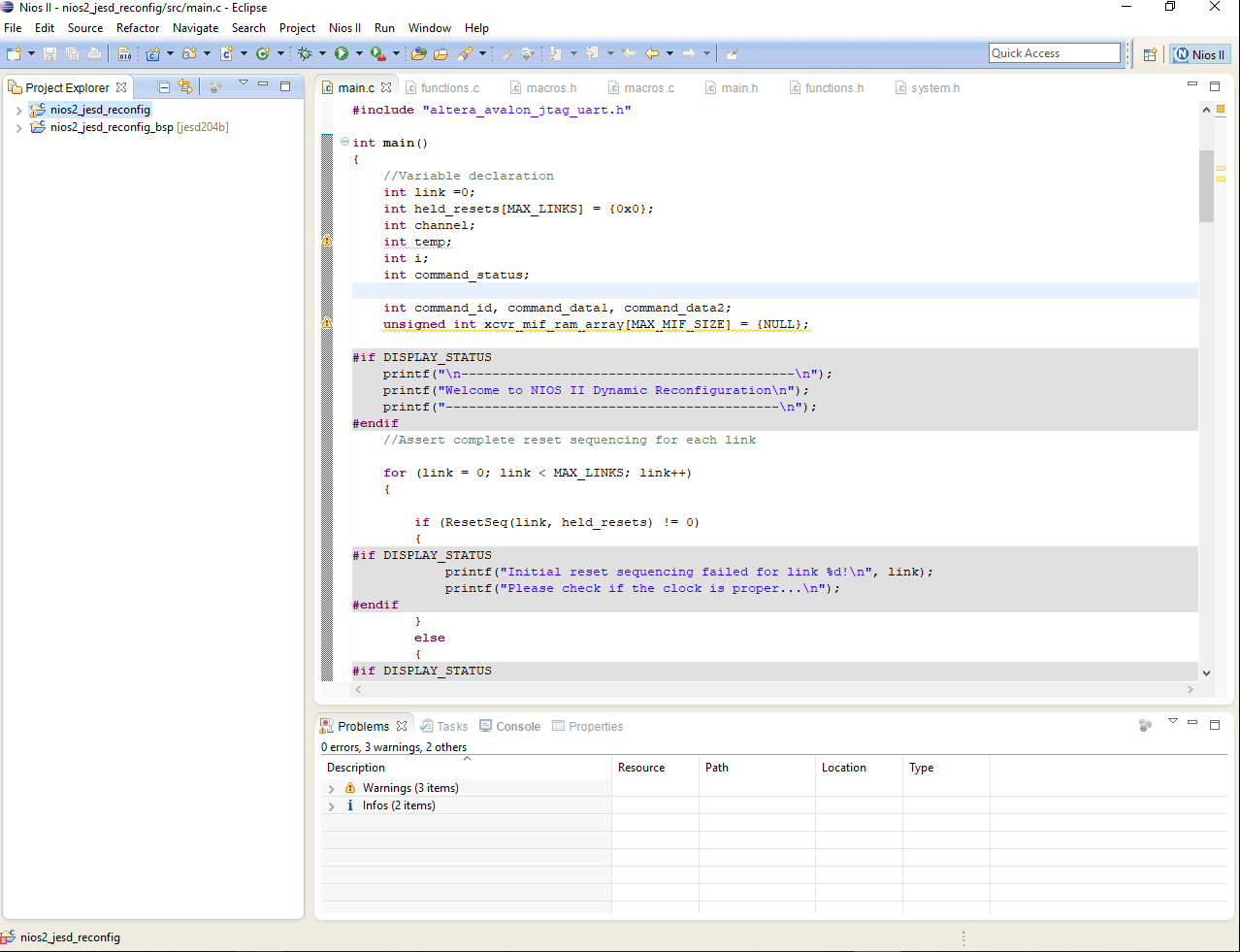
1. Every time User clicks on ‘Send’ or ‘Capture’ in HSDC Pro GUI, Software calculates lane rate based on Sampling rate entered in HSDC Pro and chooses a MIF file for the targeted line rate. The file is then parsed and the config data is sent to FPGA through FX3->I2C interface. In Firmware, I2C to Avalon master writes the MIF values to an on chip RAM ‘MIF\_ram’ component in QSYS.

Refer ‘NIOS2 Command Structure’ Excel sheet to know about MIF RAM Structure, linked in references section

1. HSDC Pro Software Issues commands to NIOS, to trigger the lane rate reconfiguration
2. Once the lanerate reconfig command is received, NIOS reads the MIF config values from the RAM memory and does dynamic reconfiguration of PHY IP and ATX PLL.

NIOS project can be opened in Quartus tool itself, with Tools->NIOS II Software Build Tools for Eclipse option and user can input the codes path as \‘Relative path of Project’\ip\software

NIOS project gets opened in Eclipse and the window will appear like below



The command used for dynamic reconfiguration of ATX PLL and PHY IP is ‘LANERATE\_RECONFIGURATION’ Following are the command registers related to Lanerate reconfiguration. NIOS command Base Addr-0x140000

|  |  |  |
| --- | --- | --- |
|  | Offset Address | Value |
| Command ID | 0x04 | 0x01 |
| Command Data1 | 0x08 | Tx reconfig - 0x01  Rx reconfig - 0x02  Both - 0x03 |
| Command Data2 | 0x0C | - |
| Command Trigger | 0x0 | 0x01 |

HSDC Pro DLL writes the command values to respective address in Nios2\_reg\_ctrl\_bram.

**Reconfig process is implemented in ‘Reconfig’ NIOS function** (available in Functions.c tab) and this gets called once the ‘LANERATE\_RECONFIGURATION’ command is received from SW.

Please refer Chapter6 and Chapter7 of Arria10 Transceiver PHY User Guide for entire reconfiguration and user calibration process of PHY IP and ATX PLL

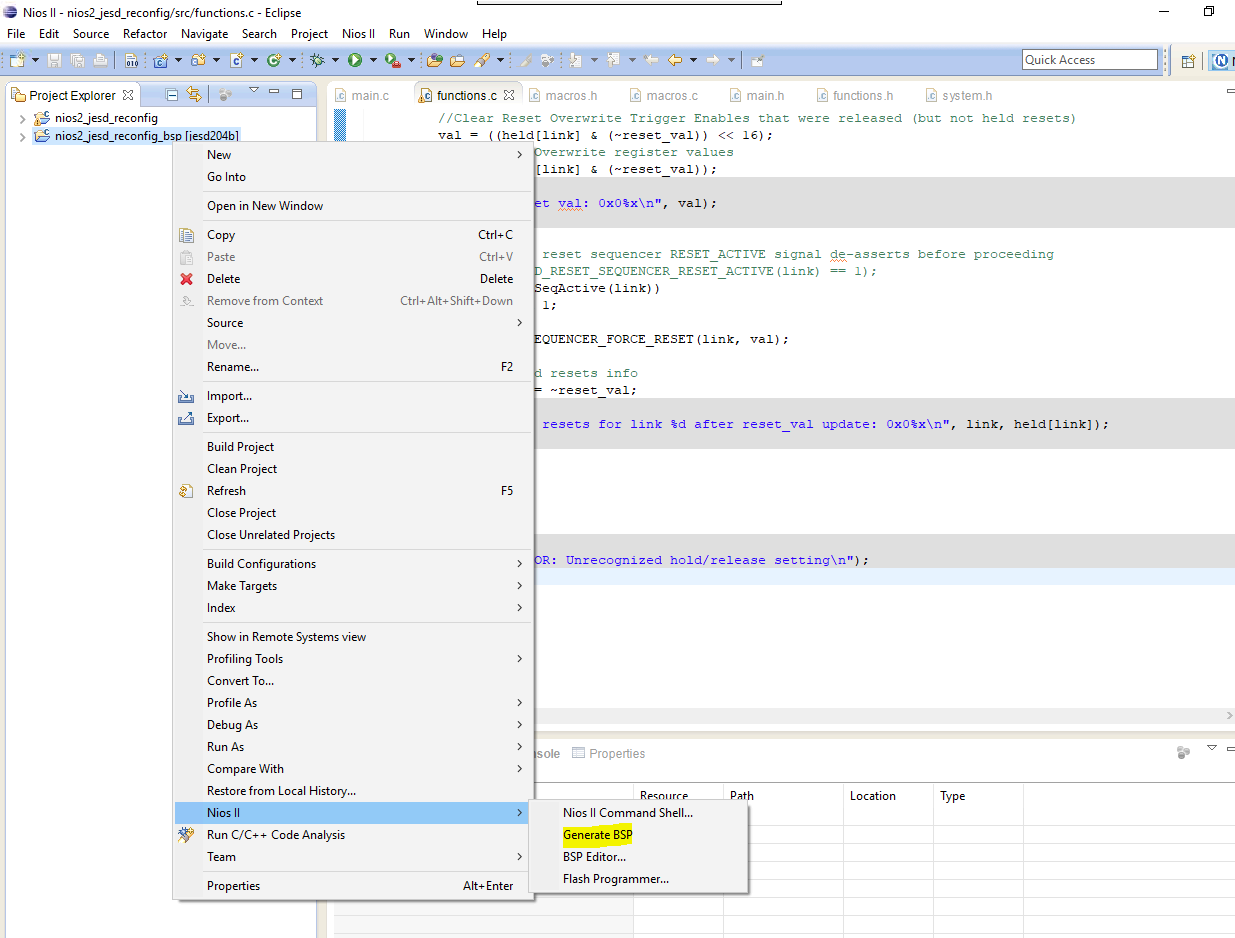
Register writes to the IP always has to be read-modify-write (RMW) as some bits are reserved in the IP for future use. Register Read Write is implemented in ‘IORMW\_XCVR\_ATX\_PLL\_A10\_REG’ and ‘IORMW\_XCVR\_NATIVE\_A10\_REG’ macros of NIOS.

Once the register writes (to re-configure for different lane rate) is done, ATX PLL and TX PMA requires calibration. Steps followed in user calibration are as per Chapter 7 of Transceiver PHY User Guide. ‘UserCalibration’ function in NIOS does it. It takes care of the ‘Arbitration’ request to access internal configuration bus used by transceiver (xcvr) channels and release of the same

Once calibration is over, xcvr link & frame resets needs to be asserted and de-asserted. ‘Reset Sequencer’ (a QSYS IP) is used to handle these resets and is controlled by NIOS through Avalon Memory Mapped interface. NIOS forces xcvr, link and frame resets using ‘ResetForce’ & ‘Reset\_X\_L\_F\_Release’ functions. Reset Sequence to be followed for assert/de-assert resets is mentioned in JESD204B IP Core Design Example User Guide (page 68)

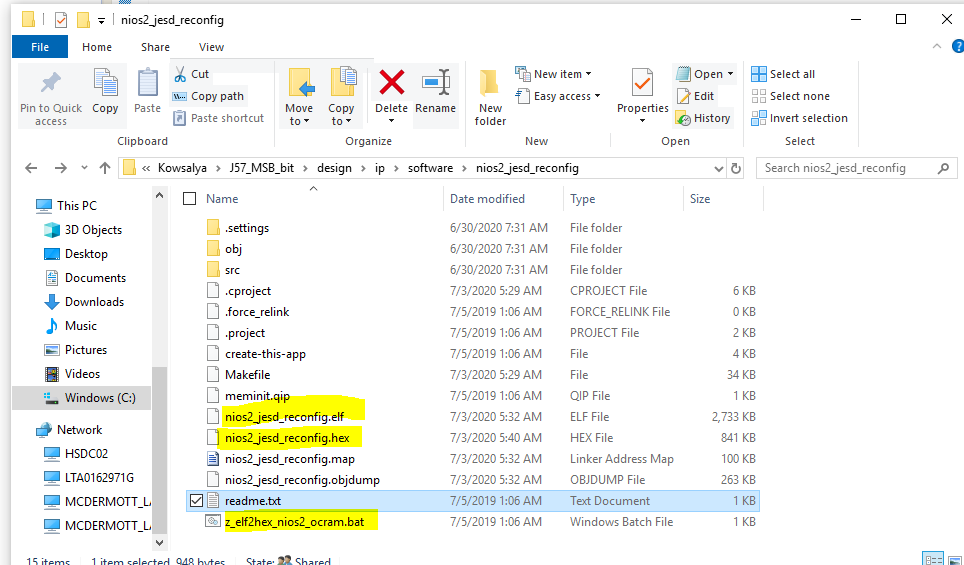
### Recompiling NIOS Codes

If any of the NIOS files are edited, user has to generate board support package files (BSP) first using Generate BSP option below and then right click nios2\_jesd\_reconfig->Build Project



Note that by recompiling the project, only the nios2\_jesd\_reconfig.elf file in below path will get updated and we need to run the z\_elf2hex\_nios2\_ocram.bat file to update nios2\_jesd\_reconfig.hex file. Hex file is the one that gets included in FW compilation

Files Path: \\*Relative Project Path\* \ip\software\nios2\_jesd\_reconfig



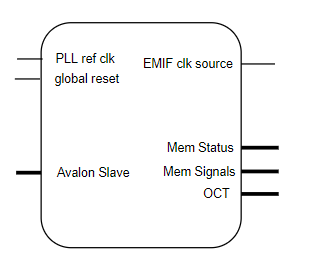
If the z\_elf2hex\_nios2\_ocram.bat file throws unrecognized commands error, please run the bat file commands in NIOS II Command shell available in Quartus 16.1 installed path- C:\intelFPGA\16.1\nios2eds\Nios II Command Shell.bat

Note, we need to change the directory in command shell to the path where z\_elf2hex\_nios2\_ocram.bat file is located

## External Memory Interface (EMIF)

The design uses single instance of Intel’s EMIF IP to interface with DDR4 memory ‘IS43QR16256A-083RBL’ of 2400 MT/s speed grade. There are 4 DDR4 chips available in J57 EVM each of 4Gb making a total 16Gb (2GB). The interface is quarter rate with a data width of 512. It can support clock speeds up to 300MHz. A 100MHz external reference clock is provided via differential pair pins [K6 L6] to the PLL inside the controller

The interface is as shown below. EMIF IP Memory settings are the recommended settings for the specific memory part- http://www.issi.com/WW/pdf/43QR16256A-85120A.pdf

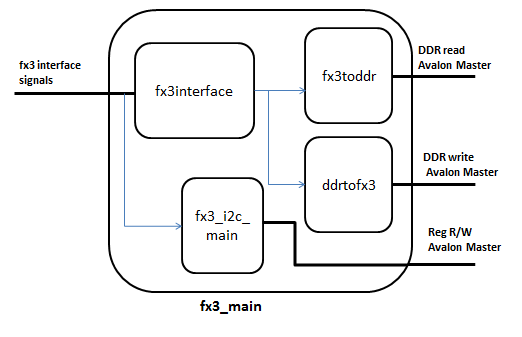


In case of transceiver mode, if the DDR memory is used, it is shared by both data capture and generation modules in which case only half of the memory is available for each. Also the throughput is reduced due to parallel read and write transactions. Whereas in non- transceiver mode, entire DDR memory 2GB size is available for either capture or generation storage

## FX3 Interface (CYUSB301X)

### FX3 Main Module

FX3 modules are the only components placed outside Qsys and its output Avalon Slave/Master interfaces are imported inside Qsys. FX3 Main has the fx3interface, fx3toddr, ddrtofx3 and fx3\_i2c\_main as sub-modules as shown below. It has three Avalon masters two for memory read and write and one for register control. It also has fx3 interface signals both I2C signals and Synchrous slave interface signals (fast parallel 32b interface) from the FX3 controller chip connected to it. This module generates and sends the fx3 pclk to FX3 chip.



Fx3 I2C Register R/W Avalon master is mapped to a custom module ‘export\_avmm\_intf’ having Avalon slave interface in Qsys. Memory Read and write Avalon masters are mapped to Avalon-MM Pipeline bridges ‘adc\_mm\_bridge\_0’ and ‘dac\_mm\_bridge\_0’ instances respectively in Qsys.

The fx3 interface module has two state machines, one for stream data in from fx3 and another for stream data out to fx3 to handle the Synchronous Slave FIFO Interface. Refer the FX3 application note “Designing with the EZ-USB FX3 Slave FIFO Interface” AN65974” for the implementation details, also linked in the references section below. This module gets the ADC and DAC start pulses from the fx3ctrl module which acts as a register file for fx3. It also sends control lines and 32bit data signals to fx3toddr and ddrtofx3 module.

The fx3toddr module has a state machine to write data to memory through Avalon Master Interface. It has a FIFO to store and convert 32b data input from the fx3interface to 512bit with FIFO depth of 256 words.

The ddrtofx3 module has a state machine to read data from memory through Avalon Master Interface. It has a FIFO which stores the 512b data from the memory and outputs 32bit to the fx3interface module with FIFO depth of 256 words.

The fx3\_i2c\_main module is connected to the fx3 i2c signals. It has Avalon Master to write and read from registers based on the i2c command given. The i2cslave module will convert the i2c signals to appropriate control signals and issues it to write\_master module. This write\_master module is connected to Avalon bus and it will write or read to FX3 register control module and other Avalon slaves inside Qsys

### FX3 Register Control

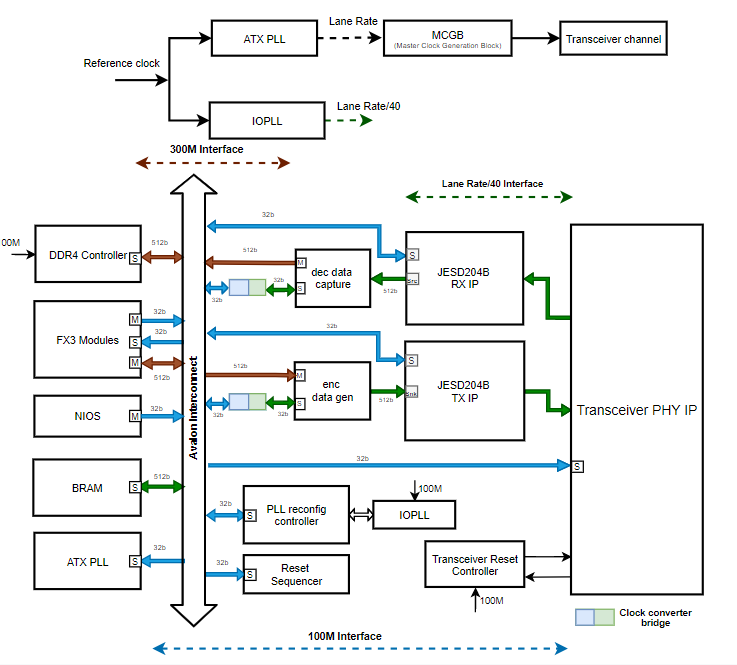
This module has an Avalon slave interface connected to the Avalon bus and holds the FX3 registers. ADC start pulse to initiate memory to FX3 transfers and DAC start pulse to initiate FX3 to memory transfers are generated in this module. It also holds a register for the data length, number of 32b words to be written or read back from memory

## Clocking Architecture

The core of the FPGA can be divided broadly into 2 regions the fabric, and the transceivers. In Arria10 device there are 24 transceiver channels grouped into 4 banks of 6 channels each. There is one fPLL, one ATX PLL and a master clock generation block (MCGB) for every 3 transceiver channels. There is also a local clock generation block (LCGB) and clock data recovery unit (CDR) in every channel. The CDR unit can function as a Clock Multiplier Unit (CMU PLL) instead of clock recovery to generate high speed transmitter clock if needed. In addition, clocks from FPGA fabric can be routed into/out of the transceivers. Also, the transceiver channels forward parallel output clock, in TX case tx\_clkout to the FPGA fabric to clock the transmitter data and control signals and in RX case rx\_clkout (derived from recovered clock) to clock the receiver data and status signals in FPGA fabric. There is a MUX to use either FPGA fabric clock (core clock) or the transceiver generated parallel clock for the FIFO used in PHY PCS layer

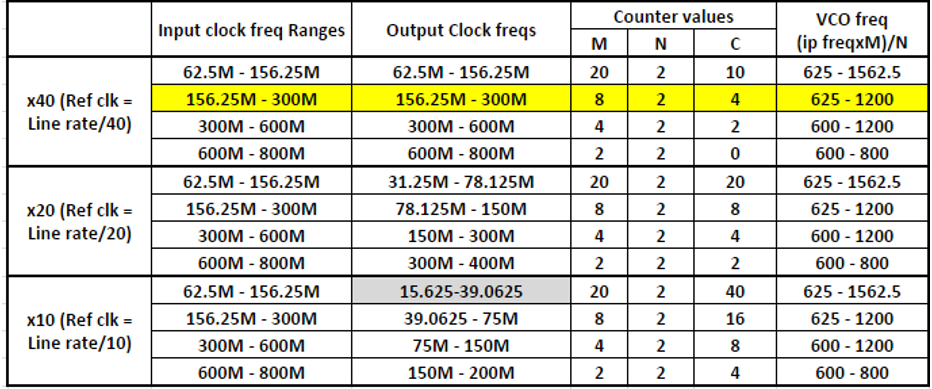
There are 3 clock domains present in the design as shown in below diagram

* All configuration interfaces are clocked at 100MHz provided by the on-board oscillator
* The JESD204B Base IP is clocked at lane rate/40 (link clock) where lane rate is the SERDES data rate and all data capture and generation modules run with link clock
* The data interface to the DDR memory interface is clocked at a fixed 300M. Since the controller is quarter rate, the external memory runs with DDR clock of 4x300 = 1200M



### RX SERDES Clocking Structure:

In the RX path, high speed serial clock is recovered from RX SERDES lanes by CDR unit and the parallel clock (rx\_link\_clk) used in PHY PCS layer is sourced by an IOPLL in FPGA fabric. IOPLL generates the lane rate/40 clock (core/link clock) and is connected to the Avalon bus through IOPLL reconfig controller. This way, HSDC software can dynamically configure PLL to generate x40 clock always irrespective of the incoming reference clock. It receives clock input from the reference clock pins [FMC-D4/D5, FPGA- AD28/AD27]. The default m, n and c counter settings of IOPLL are [4, 2, 2] with a reference clock input of 375M. HSDC software modifies m,n,c values dynamically through the Avalon interface of PLL reconfig controller. It is controlled through the FX3-> I2C Avalon master. Reference clock from the device EVM through FMC is expected to be either x40, x20 or x10 based on the lane rates. Below table gives the expected reference clock frequencies from device across different lane rates that doesn’t cause VCO input frequency to go out of range (expected range 600M – 1562.5M) and the m, n and C counter values written by HSDC DLL



**Limitation: ‘**quartus.ini’ with cpll\_disable\_oport\_rotation=on parameter is added in the project directory as recommended by Intel team due to issue seen in IOPLL reconfig controller. Issue is in some of the firmware compilations, the C counter value was not getting configured correctly

### TX SERDES Clocking Structure:

In the TX path, high speed serial clock is sourced by ATX PLL and the parallel clock (tx\_link\_clk) used in PHY PCS layer is sourced by the IOPLL in FPGA fabric. As mentioned above, IOPLL generates the lane rate/40 clock and is dynamically reconfigured by HSDC software. ATX PLL has an Avalon interface and is configured dynamically by NIOS. Clock input for ATX PLL also comes from the reference clock pins [FMC-D4/D5, FPGA- AD28/AD27] and the high speed serial clock reaches transceivers through master clock generation block and x6/xN transmitter clock network

Default ATX PLL settings: Ref clock- 375M, PLL output frequency- 7500M and Data rate- 15000M

MIF files for each of the targeted lane rates is generated and ATX PLL counter settings are stored. These files are available in HSDC Pro Software in the following path of J57revE Details Folder

C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J57revE Details\MIF Files

Every time User clicks on ‘Send’ in HSDC Pro GUI, Software calculates lane rate based on the Sampling rate entered in HSDC Pro and chooses a MIF file for the targeted line rate. The file is then parsed and the config data is sent to FPGA through FX3->I2C interface. In Firmware, I2C to Avalon master writes the MIF values to an on chip RAM ‘MIF\_ram’ component in QSYS. NIOS reads the MIF file content and writes the data to ATX PLL through Avalon interface

## Reset Module

This module ‘export\_clk\_reset’ helps with synchronous de-assertion of the external board reset with respect to different clock domains. The board reset is asynchronous in nature and it has to be synchronously de-asserted. There are six resets de-asserted with respect to DDR clock and they are being used by the ADC & DAC MM bridges of FX3 modules, Data capture & Data generation modules and their respective MM bridges. Similarly there are resets de-asserted with respect to rx link clock and tx link clock. These are used by the data capture & data generation modules and their respective MM bridges

## Register Control

This module holds the Firmware IID, memory type and Firmware type register, these registers are of READ only type. Firmware IID is used by HSDC software to update the interface name in GUI. Memory type was initially added to indicate if the data transfer is using fast 32b parallel bus (required for DDR4 external memory) or the slow I2C interface (mostly for the On-chip BRAM memory). Later on, only fast 32b parallel transfer is used for both BRAM and DDR and I2C interface was never used for data transfer and this parameter is not used in recent FW builds. Firmware type indicates maximum lanes supported either 8L or 16L used by the HSDC software in DLL layer

# Different Firmware Builds

Following firmware files are maintained for TSW14J57revE platform in HSDC Pro. All of the FWs use the same firmware architecture as explained in this design document except for some minor changes. Please refer below for more details:

1. TSW14J57revE\_16L\_DDR\_XCVR\_FIRMWARE
2. TSW14J57RevE\_16L\_XCVR\_ADCBRAMDACDDR
3. TSW14J57RevE\_16L\_XCVR\_ADCDDRDACBRAM
4. TSW14J57revE\_BRAM\_RxOnly\_16L\_FIRMWARE
5. TSW14J57revE\_BRAM\_RxOnly\_16L\_trig\_FIRMWARE
6. TSW14J57revE\_DDR\_RxOnly\_L8\_Reconfig\_FIRMWARE
7. TSW14J57revE\_ADCBRAM\_DACDDR\_L8\_Reconfig\_FIRMWARE
8. TSW14J57revE\_DDR\_XCVR\_FIRMWARE
9. TSW14J57RevE\_16L\_XCVR\_ADCBRAMDACDDR\_TIDA\_10132
10. TSW14J57REVE\_CER\_FIRMWARE

## 16L FW builds:

### TSW14J57RevE\_16L\_DDR\_XCVR\_FIRMWARE

#### Description:

Firmware supports 16L modes for both ADC and DAC devices and uses DDR4 external memory of 2GB size for both ADC capture and DAC generation. Lane values of 1,2,4,8 and 16 are tested extensively with devices and expected to work fine. L values not covered in [1,2,4,8,16] are coerced to an upper number (out of 1,2,4,8 & 16) and the data from in-active lanes are discarded in HSDC Pro through INI parameter ‘Bit Packing Pattern’ (applies to both ADC and DAC INI file). Even then, lane values 8 <L<16 doesn’t work correctly with this firmware as the lane power down logic is not handled properly but it is fixed in ‘TSW14J57RevE\_16L\_XCVR\_ADCDDRDACBRAM’ firmware. Another point to note is since the DDR memory is split by half and shared between TX and RX, there will be throughput issues when operated at higher lane rates. Features added to enhance the throughput are mentioned below. Please note firmware supports Hardware and Software trigger modes for ADC capture but SYSREF based trigger mode is not yet implemented. And none of the trigger modes are implemented for DAC generation.

TSW14J57 EVM (with Arria10 GX Speed grade2 FPGA) transceivers supports a maximum of 15Gbps SERDES Data rate. DDR4 on-board memory theoretical throughput is 153.6Gbps (300M \* 512b). Assuming 70% efficiency of DDR, practical throughput possible is 107.52Gbps (theoretical \* 0.7). With this throughput, for 8L modes max lane rate achievable is 15G but for 16L modes max lane rate possible is 8.4G only. Using DAC BCM\* feature for 16L modes further reduces the max lane rate by half to 4.2G.

To support higher lane rates and enhance the DDR throughput, features like ‘BCM Pulse mode’ and ‘Auto Duplicate First Channel data’ are added in this Firmware.

#### BCM Pulse Mode:

‘BCM Pulse Mode’ uses Firmware logic to generate a pulse of configurable width on the BCM SMA pin instead of user loading the pattern through the csv file with DAC data in HSDC GUI. User has provisions to configure the pulse start and stop index using DAC INI parameters. Please refer the ‘BCM Pulse Mode.docx’ in the Supports folder for more details, linked in the references section below

#### Auto Duplicate First Channel Data:

‘Auto Duplicate First Channel data’ feature duplicates one channel data (the first channel) to all channels in firmware before sending them to JESD Base IP which in turn sends on the TX SERDES lanes. With this feature, HSDC Pro SW needs to write only the first channel data to DDR memory and is duplicated for other channels by firmware. This greatly reduces the amount of DAC data stored in memory and also reduces the memory read and write transactions which in turn enhances the throughput. Please refer the ‘TX Auto Duplicate first channel data.docx’ in the Supports folder for more details, linked in the references section below

Note: Current Architecture for BCM feature is such that BCM pattern gets written along with DAC data to the same DDR memory but is read back and sent on SMA pin instead of JESD link. BCM pattern occupies the same size as DAC data, so the memory available for valid DAC data is reduced by half and the throughput also reduced by half as the pattern gets read back along with valid DAC data for every read transaction. Refer the ‘BCM Feature.docx’ in the Supports folder for more details

#### LED Status:

Please see below description of the on-board user LED signals for this FW build. Please note J57 platform User LEDs are active LOW

|  |  |
| --- | --- |
| User LEDs | Functionality |
| D1 | Indicates TX SYNC is established when OFF |
| D2 | Indicates presence of TX link clock and JESD link is established when blinking |
| D3 | Indicates RX SYNC is established when OFF  (and the reverse if incase RX SYNC pin P/N is swapped in device) |
| D4 | Indicates presence of RX link clock and JESD link is established when blinking |
| D5 | Indicates presence of RX link clock when blinking |
| D6 | Indicates presence of TX link clock when blinking |
| D7 | DDR4 calibration successful and completed when off |
| D8 | DDR4 calibration failed when off |

### TSW14J57RevE\_16L\_XCVR\_ADCBRAMDACDDR

#### Description:

Firmware supports 16L modes for both ADC and DAC devices and uses DDR4 external memory of 2GB size for DAC generation and BRAM of 256KB size for ADC capture. The limitations on L value mentioned for TSW14J57revE\_16L\_DDR\_XCVR\_FIRMWARE applies to this firmware as well. Also firmware supports Hardware and Software trigger modes for ADC capture but SYSREF based trigger mode is not yet implemented. And none of the trigger modes are implemented for DAC generation.

This firmware supports ‘Frequency Hopping feature’ developed and tested with AFE74xx in HSDC Pro. It does a high speed SPI write of 40Mhz, and between SPI writes it supports a configurable delay and trigger width that ranges from ns to ms. Please refer the ‘Frequency Hopping’ documents available in ‘Supports folder’ for further details. Firmware also supports pulse generation on SMA pin whenever one of the TX SERDES lanes are powered down. This was done as part of the JESD204B Error Injection feature addition. Please refer the ‘JESD204B Error Injection – Summary.docx’ placed in the ‘Supports folder’ for more details

#### LED Status:

Please see below description of the on-board user LED signals for this FW build. Please note J57 platform User LEDs are active LOW

|  |  |
| --- | --- |
| User LEDs | Functionality |
| D1 | Indicates TX SYNC is established when OFF |
| D2 | Indicates presence of TX link clock and JESD link is established when blinking |
| D3 | Indicates RX SYNC is established when OFF  (and the reverse if incase RX SYNC pin P/N is swapped in device) |
| D4 | Indicates presence of RX link clock and JESD link is established when blinking |
| D5 | Indicates presence of RX link clock when blinking |
| D6 | Indicates presence of TX link clock when blinking |
| D7 | DDR4 calibration successful and completed when off |
| D8 | DDR4 calibration failed when off |

### TSW14J57RevE\_16L\_XCVR\_ADCDDRDACBRAM

#### Description:

Firmware supports 16L modes for both ADC and DAC devices and uses DDR4 external memory of 2GB size for ADC capture and BRAM of 256KB size for DAC generation. As mentioned in ‘TSW14J57revE\_16L\_DDR\_XCVR\_FIRMWARE’ firmware, lane values of 1,2,4,8 and 16 are tested extensively with devices and expected to work fine. L values not covered in [1,2,4,8,16] are coerced to an upper number (out of 1,2,4,8 & 16) and the data from in-active lanes are discarded in HSDC Pro through INI parameter ‘Bit Packing Pattern’ (applies to both ADC and DAC INI file). Also firmware supports Hardware and Software trigger modes for ADC capture but SYSREF based trigger mode is not yet implemented. And none of the trigger modes are implemented for DAC generation.

#### LED Status:

Please see below description of the on-board user LED signals for this FW build. Please note J57 platform User LEDs are active LOW

|  |  |
| --- | --- |
| User LEDs | Functionality |
| D1 | Indicates TX SYNC is established when OFF |
| D2 | Indicates presence of TX link clock and JESD link is established when blinking |
| D3 | Indicates RX SYNC is established when OFF  (and the reverse if incase RX SYNC pin P/N is swapped in device) |
| D4 | Indicates presence of RX link clock and JESD link is established when blinking |
| D5 | Indicates presence of RX link clock when blinking |
| D6 | Indicates presence of TX link clock when blinking |
| D7 | DDR4 calibration successful and completed when off |
| D8 | DDR4 calibration failed when off |

### TSW14J57RevE\_16L\_XCVR\_ADCBRAMDACDDR\_TIDA\_10132

#### Description:

Same as the TSW14J57RevE\_16L\_XCVR\_ADCBRAMDACDDR firmware with changes on TX and RX SYNC lines done specifically for TIDA- 10132 EVM. TIDA has two AFE76xx DUTs, AFE1 and AFE2 that needs to be interfaced with a single J57 capture card. To use both the AFEs together, we planned to test 8L modes of AFEs with the normal SYNC lines TX\_SYNC FMC F10/F11 and RX\_SYNC FMC G12/G13 routed to AFE1 and use the alternate SYNC lines TX\_ALT\_SYNC FMC F19/F20 and RX\_ALT\_SYNC FMC H31/H21 to AFE2. In the firmware RX SYNC signal out of the JESD Base IP is sent to both normal and Alternate lines and a logic is added on TX side to select either normal or the alternate SYNC or combine both based on ‘txsyncselect’ DAC INI parameter. Note all the SYNC signals are LVDS signals where as in other FW builds only normal RX/TX SYNC lines are LVDS and alternate RX SYNC lines are LVCMOS 1.8V and alternate TX SYNC is not used other FW builds.

#### LED Status:

Please see below description of the on-board user LED signals for this FW build. Please note J57 platform User LEDs are active LOW

|  |  |
| --- | --- |
| User LEDs | Functionality |
| D1 | Indicates TX SYNC is established when OFF |
| D2 | Indicates presence of TX link clock and JESD link is established when blinking |
| D3 | Indicates RX SYNC is established when OFF  (and the reverse if incase RX SYNC pin P/N is swapped in device) |
| D4 | Indicates presence of RX link clock and JESD link is established when blinking |
| D5 | Indicates presence of RX link clock when blinking |
| D6 | Indicates presence of TX link clock when blinking |
| D7 | DDR4 calibration successful and completed when off |
| D8 | DDR4 calibration failed when off |

### TSW14J57revE\_BRAM\_RxOnly\_16L\_FIRMWARE

#### Description:

Firmware supports only RX operation and uses BRAM of 2MB size to store ADC captures. FW doesn’t support any of the trigger modes for capture and timing is not met. This is one of the initial FW releases and is replaceable with 16L transceiver (XCVR) FW builds mentioned above. There is minor change with respect to FW architecture, the BRAM memory instantiation is placed in ‘dec\_data\_capture\_gz’ module in this FW build where as in the latest 16L XCVR FWs, a BRAM wrapper modules is created and is placed as separate QSYS component. And BRAM memory uses I2C interface for read and write, so HSDC Pro captures will take time to reflect, only the external DDR memory had fast parallel transfer interface. But the latest 16L FWs use 32b parallel data transfer for BRAM memory as well

#### LED Status:

Please see below description of the on-board user LED signals for this FW build. Please note J57 platform User LEDs are active LOW

|  |  |
| --- | --- |
| User LEDs | Functionality |
| D1 | Indicates TX SYNC is established when OFF |
| D2 | Indicates presence of TX link clock and JESD link is established when blinking |
| D3 | Indicates RX SYNC is established when OFF  (and the reverse if incase RX SYNC pin P/N is swapped in device) |
| D4 | Indicates presence of RX link clock and JESD link is established when blinking |
| D5 | Indicates trigger input signal  (if LED debug INI parameter is 1, used to check the debug signals from NIOSII Soft- processor in FPGA) |
| D6 | DDR4 calibration successful and completed when off  (if LED debug INI parameter is 1, indicates RX link is established and data capture process is happening when OFF) |
| D7 | DDR4 calibration successful and completed when off  (if Binary Channel Mode is enabled, indicates BCM data) |
| D8 | DDR4 calibration failed when off  (if LED debug INI parameter is 1, indicates presence of SYSREF when blinking) |

### TSW14J57revE\_BRAM\_RxOnly\_16L\_trig\_FIRMWARE

#### Description:

Same as the TSW14J57revE\_BRAM\_RxOnly\_16L\_FIRMWARE build mentioned above with trigger feature added for ADC capture. Only Hardware and Software trigger modes added for capture and SYSREF based trigger mode is not implemented yet.

#### LED Status:

|  |  |
| --- | --- |
| User LEDs | Functionality |
| D1 | Indicates TX SYNC is established when OFF |
| D2 | Indicates presence of TX link clock and JESD link is established when blinking |
| D3 | Indicates RX SYNC is established when OFF  (and the reverse if incase RX SYNC pin P/N is swapped in device) |
| D4 | Indicates presence of RX link clock and JESD link is established when blinking |
| D5 | Indicates trigger input signal  (if LED debug INI parameter is 1, used to check the debug signals from NIOSII Soft- processor in FPGA) |
| D6 | DDR4 calibration successful and completed when off  (if LED debug INI parameter is 1, indicates RX link is established and data capture process is happening when OFF) |
| D7 | DDR4 calibration successful and completed when off  (if Binary Channel Mode is enabled, indicates BCM data) |
| D8 | DDR4 calibration failed when off  (if LED debug INI parameter is 1, indicates presence of SYSREF when blinking) |

### TSW14J57REVE\_CER\_FIRMWARE

#### Description:

This firmware build was mainly developed for CER feature and has a slightly different architecture. Please refer the “TSW14J57 CER Firmware.docx” placed parallel to this document for more details

Please see below description of the on-board user LED signals for this FW build. Please note J57 platform User LEDs are active LOW

#### LED Status:

|  |  |
| --- | --- |
| User LEDs | Functionality |
| D1 | Indicates TX SYNC is established when OFF |
| D2 | Indicates presence of TX link clock and JESD link is established when blinking |
| D3 | Indicates RX SYNC is established when OFF  (and the reverse if incase RX SYNC pin P/N is swapped in device) |
| D4 | Indicates presence of RX link clock and JESD link is established when blinking |
| D5 | Indicates trigger input signal |
| D6 | DDR4 calibration successful and completed when off  (if LED debug INI parameter is 1, indicates RX link is established and data capture process is happening when OFF) |
| D7 | DDR4 calibration successful and completed when off  (if Binary Channel Mode is enabled, indicates BCM data) |
| D8 | DDR4 calibration failed when off  (if LED debug INI parameter is 1, indicates presence of SYSREF when blinking) |

## 8L FW builds:

### TSW14J57revE\_DDR\_RxOnly\_L8\_Reconfig\_FIRMWARE

#### Description:

Firmware supports only RX operation and maximum of 8 lanes only supported. Only Lane values of 1, 2, 4 and 8 are expected to work fine and other L values not supported. Also firmware doesn’t support individual SERDES Lane inversion (P/N swapping). None of Trigger mode supports is available. Uses DDR memory of 2GB for ADC capture. This is one of the initial FW releases, timing is not met in this build and is replaceable with 16L transceiver (XCVR) FW builds mentioned above.

#### LED Status:

Please see below description of the on-board user LED signals for this FW build. Please note J57 platform User LEDs are active LOW

|  |  |
| --- | --- |
| User LEDs | Functionality |
| D1 | Indicates RX SYNC is established when ON  (and the reverse if incase RX SYNC pin P/N is swapped in device) |
| D2 | Indicates presence of RX link clock when blinking |
| D3 | Indicates presence of device clock when blinking |
| D4 | Indicates presence of SYSREF when blinking |
| D5 | Indicates presence of RX link clock when blinking |
| D6 | DDR4 calibration successful and completed when off |
| D7 | DDR4 calibration successful and completed when off |
| D8 | DDR4 calibration failed when off |

### TSW14J57revE\_ADCBRAM\_DACDDR\_L8\_Reconfig\_FIRMWARE

#### Description:

Firmware supports both TX and RX operation and maximum of 8 lanes only supported. Only Lane values of 1, 2, 4 and 8 are expected to work fine and other L values not supported. Also firmware doesn’t support individual SERDES Lane inversion (P/N swapping) both TX and RX. None of Trigger mode supports is available for both TX and RX. Uses DDR memory of 2GB for DAC generation and BRAM memory of 512KB for ADC capture. This is one of the initial FW releases, timing is not met in this build and is replaceable with 16L transceiver (XCVR) FW builds mentioned above

#### LED Status:

Please see below description of the on-board user LED signals for this FW build. Please note J57 platform User LEDs are active LOW

|  |  |
| --- | --- |
| User LEDs | Functionality |
| D1 | Indicates TX SYNC is established when OFF |
| D2 | Indicates presence of TX link clock and JESD link is established when blinking |
| D3 | Indicates RX SYNC is established when OFF  (and the reverse if incase RX SYNC pin P/N is swapped in device) |
| D4 | Indicates presence of RX link clock and JESD link is established when blinking |
| D5 | Indicates the trigger input signal |
| D6 | DDR4 calibration successful and completed when off |
| D7 | DDR4 calibration successful and completed when off |
| D8 | DDR4 calibration failed when off |

### TSW14J57revE\_DDR\_XCVR\_FIRMWARE

#### Description:

Firmware supports both TX and RX operation and maximum of 8 lanes only supported. Lane values of 1,2,4 and 8 are tested extensively with devices and expected to work fine. L values not covered in [1,2,4,8] are coerced to an upper number (out of 1,2,4 & 8) and the data from in-active lanes are discarded in HSDC Pro through INI parameter ‘Bit Packing Pattern’ (applies to both ADC and DAC INI file). FW shares the DDR memory of 2GB between ADC Capture and DAC generation each using 1GB, hence the throughput limitations mentioned for TSW14J57RevE\_16L\_DDR\_XCVR\_FIRMWARE applies here as well, please refer above. Individual SERDES Lane inversion (P/N swapping) can be corrected in this build through ‘Enable Individual Lane Inversion’ INI parameter like the 16L latest FW builds. None of Trigger mode supports is available for both TX and RX. This is one of the initial FW releases, timing is met in this build but is replaceable with 16L transceiver (XCVR) FW builds mentioned above

#### LED Status:

Please see below description of the on-board user LED signals for this FW build. Please note J57 platform User LEDs are active LOW

|  |  |
| --- | --- |
| User LEDs | Functionality |
| D1 | Indicates TX SYNC is established when OFF |
| D2 | Indicates presence of TX link clock and JESD link is established when blinking |
| D3 | Indicates RX SYNC is established when OFF  (and the reverse if incase RX SYNC pin P/N is swapped in device) |
| D4 | Indicates presence of RX link clock and JESD link is established when blinking |
| D5 | Indicates presence of RX link clock when blinking |
| D6 | Indicates presence of TX link clock when blinking |
| D7 | DDR4 calibration successful and completed when off |
| D8 | DDR4 calibration failed when off |

# References:

1. \\*\TI HSDC KT\TSW14J57\Reference Documents\Other Documents\I2C packet Structure.xlsx
2. \\*\TI HSDC KT\TSW14J57\Reference Documents\Other Documents\JESD204B\_IP\_dynamic\_reconfig\_3Sep15\_TI.pptx
3. \\*\TI HSDC KT\TSW14J57\Reference Documents\Other Documents\NIOS2 Command Structure.xlsx
4. \\*\TI HSDC KT\TSW14J57\Reference Documents\Other Documents\TSW14J56 RevD Trigger Modes.docx
5. \\*\TI HSDC KT \TSW14J57\Supports\BCM Pulse Mode
6. \\*\TI HSDC KT \TSW14J57\Supports\Auto Duplicate DAC First Channel Data
7. AN729 ‘Implementing JESD204B IP Core System Reference Design with Nios II Processor as Control Unit’ was taken as reference to implement the NIOS codes
8. Refer Chapter6 and Chapter7 of Arria10 Transceiver PHY User Guide for entire reconfiguration and user calibration process of PHY IP and ATX PLL
9. Refer JESD204B IP Core Design Example User Guide (page 68) for the reset sequence to be followed for assert/de-assert xcvr, link and frame resets
10. “Designing with the EZ-USB FX3 Slave FIFO Interface” AN65974- Application note from Cypress FX3